has applied a new reference and cited different portions of one of the references applied in the previous Action in order to support a new ground of rejection. However, applicants' amendment did not necessitate the new ground of rejection. Since the subject matters of all the current claims had already been presented prior to the first Action, the Examiner should have made this rejection in the first Action as well. Accordingly, the finality of the Action should be withdrawn.

Claims 4, 5, 14 and 15 have been rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,686,754 (Choi). This rejection is respectfully traversed.

As applicants explained in the previous amendment, claim 4 includes a resistance layer of a second conductivity and a pair of electrode pad layers of the second conductivity type formed at both ends of the resistance layer. Accordingly, the resistance layer has the same conductivity type as that of the two electrode pad layers. This is a requirement for a resistor element, such as that of claim 4, to operate in a semiconductor device. On the other hand, Choi's device has two electrode pad layers 60, 61 of an N type and a P type region 64. The Examiner cites "the thin layer between a pair of electrode pad layer 60/61" as the resistance layer of claim 4. However, this thin layer is a channel layer of Choi's MOS-FET device, and is a part of the P type region 64. Besides, in a MOS-FET device, the channel layer 64 has to be of a conductivity type different from the conductivity type of the contact regions 60, 61, as persons of ordinary skill in the art would have known. Choi's channel layer has a conductivity type that is different from that of the contact regions 60, 61.

Thus, Choi does not teach or suggest the resistance layer and the pair of electrode pad layers of claim 4, which have the same conductivity type. All other claims depend from claim 4. Accordingly, the rejection of claims 4, 5, 14 and 15 should be withdrawn.

Claims 4, 5, 14 and 15 have been rejected under 35 USC 102(e) as being anticipated by U.S. Patent Publication No. 2002/0057187 (Sanfilippo). This rejection is respectfully traversed.

This application claims priority from Japanese Patent Application No. 2000-321250, which was filed on October 20, 2000. Since this Japanese application was filed before Sanfilippo, which was filed on December 22, 2000, it removes Sanfilippo as a prior art reference. A sworn translation of Japanese Patent Application No. 2000-3212500 is filed with this response.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **492322002200**.

Respectfully submitted,

Dated: April 21, 2003 By: _____

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I hereby certify that this translation is a literal translation of a Japanese Patent Application No. 2000-321250.

Toshio Matsuoka

Toshio Matsuoka

April 21, 2003

[Document Name] Specification

[Title of the Invention] Semiconductor Device and Manufacturing Method Therefor

[CLAIMS]

1. A semiconductor device comprising:

a resistance layer formed on a semiconductor substrate of a first conductivity type and of a second conductivity type, one end of said resistance layer being adapted to have a first voltage applied thereto, another end of said resistance layer being adapted to have a second voltage applied thereto;

an insulating film formed on the resistance layer; and

a resistance bias electrode layer comprising a silicon layer formed on the insulating film;

wherein the device is configured so that voltage dependence of a resistance of the resistance layer is reduced by adjusting the voltage applied to the resistance bias electrode layer.

2. The semiconductor device of claim 1, wherein the voltage applied to the silicon layer is provided from the middle of the resistance layer in a longitudinal direction.

3. A method of manufacturing the semiconductor device of claim 1, comprising:

forming an insulating film and a first silicon layer on a semiconductor substrate of a first conductivity type;

selectively forming an oxidation resistant film on the first silicon layer;

forming a field oxide film by thermal oxidation;

removing the oxidation resistant film;

forming a resistance layer of a second conductivity type on a surface of the semiconductor substrate by ion implantation of an impurity of the second conductivity type penetrating through the first silicon layer and the insulating film;

forming a second silicon layer covering the whole area of the device;

forming a resistance bias electrode layer on the resistance layer through a patterning of the first silicon layer and the second silicon layer; and

forming a wiring layer for providing the resistance bias electrode layer with a predetermined voltage.

4. The method of manufacturing the semiconductor device of claim 3, wherein the wiring layer contacts with the resistance layer at the middle of the resistance layer in longitudinal direction.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

This invention relates to a semiconductor device and its manufacturing method, especially to a semiconductor device in which resistor elements are integrated on a semiconductor substrate.

[0002]

[Background Art]

Resistor elements have been used in a variety of semiconductor integrated circuits, including resistors for delay circuits, resistors for oscillator circuits, and ladder resistors for Analog-Digital converters. Figure 11 is a cross-sectional view of the structure of a prior art semiconductor device.

[0003]

On N-type semiconductor substrate 50, field oxide films 51 are formed. P^--type resistance layer 52 is formed on the surface of the N-type semiconductor substrate 50 between the field oxide films 51. Also, on both sides of the P^--type resistance layer 52, P^+-type electrode pad layers 53 and 54 are formed.

[0004]

Figure 12 shows a cross section of the semiconductor device of Figure 11 in use. The voltage VL is applied to the electrode pad layer 53, and the voltage VH is applied to the electrode pad layer 54 in the Figure. Hence, when the voltage of the N-type semiconductor substrate 50 is 0V, it is supposed that VH < VL < 0V. That is, forward bias of the P^+-type electrode pad layers 53 and 54 and the N-type semiconductor substrate 50 is prevented. Also, in terms of absolute value, voltage VH is greater than voltage VL. Therefore, electric current goes through the P^--type resistance layer 52 according to the voltage difference (VH – VL).

[0005]

[Problems to be Solved by the Invention]

When the resistance layer 52 is used as a resistor element in a semiconductor integrated circuit, it is desirable that there be no voltage dependence of the resistance value for the sake of circuit design.

[0006] However, when voltage VH is applied to the P^+-type electrode pad layer 54, the depletion layer 55 between the N-type semiconductor substrate 50 and the P^--type resistance layer 52 is expanded. Therefore, the P^--type resistance layer 52 is narrowed down, causing the change in a resistance value, which depends on the voltage VH applied to the P^+-type electrode pad layer 54. Also, when the voltage VH rises further, a pinch-off state takes place near the P^+-type electrode pad layer 54, leading to saturation of the electric current.

[0007]

This invention is directed to reducing voltage dependence as much as possible, which can simplify the design of semiconductor integrated circuits.

[0008]

[Means for Solving the Problems]

The semiconductor device of this invention has a resistance layer of a second conductivity type formed on the surface of the semiconductor substrate of a first conductivity type, where a first voltage is applied to one end of the resistance layer and a second voltage is applied to the other end, an insulating film formed on the resistance layer of the second conductivity type, and a resistance bias electrode layer comprising silicon layer on the insulating film.

[0009]

By adjusting the voltage applied to the resistance bias electrode layer, the voltage dependence of the resistance of the resistance layer of the second conductivity type can be reduced.

[0010]

The method of manufacturing the semiconductor device of this invention includes forming an insulating film and a first silicon layer on the semiconductor substrate of the first conductivity type, selectively forming a oxidation resistant film on the first silicon layer, forming a field oxide film by thermal oxidation, removing the oxidation resistant film, forming a resistance layer of the second conductivity type on the surface of the semiconductor substrate by ion implantation of the impurity of the second conductivity type penetrating through the first silicon layer and the insulating film, forming a second silicon layer covering the whole area, forming a resistance bias electrode layer on the resistance layer through the patterning of the first and second silicon layers, and forming a wiring layer for providing the resistance bias electrode layer with the predetermined voltage.

[0011]

The manufacturing method of this invention allows for the reduction of manufacturing process steps, because the first silicon layer remains intact when the field oxide film is formed and then is used as a part (that is, a lower part) of the resistance bias electrode layer.

[0012]

Furthermore, the resistance layer of the second conductivity type is formed by the ion implantation of the impurity of the second conductivity type penetrating through the first silicon layer and the insulating film. Then, the second silicon layer is deposited on the first silicon layer. Thus, the first silicon layer functions as a buffer film against the ion implantation, and the acceleration energy of the ion implantation can be reduced compared to the case in which the single silicon layer is used as the resistance bias electrode layer.

[0013]

[Description of the Invention]

Now, the semiconductor device and the manufacturing method to which this invention applies will be explained by referring to Figs 1-6. In Figs. 1-6, the region where the diffusion resistance is to be formed is shown in the right sides of the figures, and the region where P-channel MOS transistor is to be formed is shown in the left sides of the figures, respectively.

[0014]

As seen from Fig. 1, on the P-type silicon substrate 1, N-type well region 2 is formed. Also, on the P-type silicon substrate 1, a thin oxide film 3 of a thickness of 10 nm - 20 nm is formed by thermal oxidation. On this thin oxide film 3, the first polysilicon layer 4 of a thickness of 50 nm - 100 nm and the silicon nitride film (Si_3N_4) 5 of 50 nm - 100 nm are formed by an LPCVD method. Then, etching is performed selectively on the silicon nitride film 5. Here, instead of the first polysilicon layer 4, an amorphous silicon layer can be formed.

[0015]

By this, the double layer comprising the first polysilicon layer 4 and the silicon nitride film 5 remains in predetermined areas in both the P-channel MOS transistor forming region and the polysilicon resistance element forming region. Here, it is also possible to perform the etching selectively on the first polysilicon layer 4 and the silicon nitride film 5.

[0016]

Then, thermal oxidation at about 1000℃ is performed. As shown in Fig. 2, the field oxide film 6 is formed in the area where the silicon nitride film has been removed by etching. The thickness of the field oxide film 6 is about 500 nm, for example. Here, the silicon nitride film 5 functions as an oxidation resistant film. Also, the thin oxide film 3 is also called a pad oxide film, and it prevents crystal defects in the P-type silicon substrate under the so-called bird's beak of the field oxide film 6.

[0017]

Additionally, the first polysilicon layer 4 is called a pad polysilicon layer (pad silicon layer) and works to shorten the bird's beak. Usually, the thin oxide film 4 and the first polysilicon layer 4 are removed after the field oxidation. However, this manufacturing process keeps them intact and utilizes them as structural components of the resistor element as described later.

[0018]

Next, as shown in Fig. 3, a photoresist layer 7 is formed on the P-channel MOS transistor forming region after the silicon nitride film 5 is removed. Using this photoresist layer 7 as a mask, ion implantation of P-type impurity is performed penetrating the first polysilicon layer 4 and the thin oxide film 3, and the P-type resistance layer 8 is formed on the surface of the N-type well region 2. Here, the preferable condition of the ion implantation process is as follows: boron ion is used in the ion implantation, the acceleration energy is 60 KeV, and the dose is 8.5×10^{12} / cm^2.

[0019]

During the ion implantation process described above, the first polysilicon layer

4 and the thin oxide film 3 function as a buffer film against the ion implantation and prevent crystal defects on the surface of the semiconductor substrate. Also, since the first polysilicon layer 4 is relatively thin, the acceleration energy of the ion implantation can be reduced.

[0020]

Then, as shown in Fig. 4, the second polysilicon layer 9 of a thickness of 50 nm - 100 nm is deposited to cover the whole surface by an LPCVD method after the removal of the photoresist layer 7 from the P-channel MOS transistor forming region. To the second polysilicon layer 9, the doping of an impurity such as phosphorus is performed by thermal diffusion, resulting in the reduction of the resistance of the second polysilicon layer 9. Here, by causing the impurity to diffuse reaching to the first polysilicon layer 4 beneath the second polysilicon layer 9, the resistance of the first polysilicon layer 4 is also reduced.

[0021]

By this, the second polysilicon layer 9 is deposited on the first polysilicon layer 4 in the P-channel MOS transistor forming region as well as in the diffusion resistance forming region.

[0022]

Then, as shown in Fig. 5, in the predetermined area on the second polysilicon layer 9, the photoresist layer (not shown in the figure) is formed. Using this photoresist layer as a mask, the etching on the second polysilicon layer 9 and the first polysilicon layer 4 is sequentially and selectively performed.

[0023]

By this, in the diffusion resistance forming region, a resistance bias electrode 10, which consists of stacked layers of the first polysilicon layer 4 and the second polysilicon layer 8, is formed. On the other hand, in the P-channel MOS transistor forming region, a gate electrode 11, which consists of stacked layers of the first polysilicon layer 4 and the second polysilicon layer 8, is formed. Also, on the field oxide film 6, a polysilicon wiring layer (not shown in the figure) comprising the second polysilicon layer 9 (single layer) is formed.

[0024]

Furthermore, by implanting an ion such as boron, the P^+-type electrode pad layers 12, 13, the P^+-type source layer 14 and the P^+-type drain layer 15 of the P-channel MOS transistor are formed.

[0025]

Next, as shown in Fig. 6, an interlayer insulating film 16, such as a BPSG (Boro-Phospho Silicate Glass) film, is formed on the whole surface. On the P^+-type electrode pad layers 12, 13, P^+-type source layer 14 and the P^+-type drain layer 15, contact holes are formed. Through those contact holes, resistance connection electrode 17, 18, a source electrode 19, and a drain electrode 20, comprising Al layers, are formed. This completes the semiconductor device with the diffusion resistance. Although the explanation about forming an N-channel MOS transistor is omitted here, it is formed on the same silicon substrate 1 to form a CMOS structure.

[0026]

Fig. 7 is a plan view of the diffusion resistance shown in Fig. 6. A strip of P^--type resistance layer 8 extends between the P^+-type electrode pad layers 12 and 13. Reference numerals C1 and C2 denote the contact holes formed on the P^+-type electrode pad layers 12 and 13. The length of the P^--type resistance layer 8 is determined according to the desired resistance value. Also, P^--type resistance layer 8 is covered with the resistance bias electrode 10 with the thin insulating film 3 between them. This resistance bias electrode 10 is connected to the Al wiring layer 21 through the contact hole C3. A predetermined bias voltage VG is applied to the Al wiring layer 21 from a power source. By adjusting this bias voltage VG, the

expansion of the depletion layer between the P^--type resistance layer 8 and the N type well region 2 is suppressed.

[0027]

Fig. 8 is another plan view of the diffusion resistance. Here, a contact hole C4 is formed in the middle of the P^--type resistance layer 8 in longitudinal direction, and a contact hole C5 is formed on the resistance bias electrode 10. Through these contact holes C4 and C5, the P^--type resistance layer 8 and the resistance bias electrode 10 are connected by the Al wiring layer 22. In this case, the voltage taken out from the P^--type resistance layer 8 is applied to the resistance bias electrode 10. Thus, use of an additional power voltage source is not required, which is one of the advantages of this embodiment.

[0028]

Next, experimental results of the semiconductor device will be explained by referring to Figs. 9 and 10, Figs. 9 and 10 show the current-voltage characteristics and the resistance characteristics of the diffusion resistance (the difference in the voltages between both sides of the diffusion resistance being shown on the X-axis, and the electric current I and the resistance Rs being shown on the Y-axis). Here, the voltage applied to the P^+-type electrode pad layer 13 is VH, the voltage applied to the P^+-type electrode pad layer 12 is VL, and the voltage applied to the resistance bias electrode 10 is VG.

[0029]

It is defined that R = VG / (VH – VL), where R denotes the ratio of the voltage VG applied to the resistance bias electrode 10 to the voltage VH applied to the P^+-type electrode pad layers 13. According to this definition, the characteristics described above are shown for R = 0 in Fig. 9 (A), for R = 0.2 in Fig. 9 (B), for R = 0.4 in Fig. 9 (C), for R = 0.5 in Fig. 10 (D), for R = 0.6 in Fig. 10 (E) and for R = 0.8 in Fig. 10 (F).

[0030]

As shown by the above experimental results, the voltage dependence becomes smallest when R = 0.6. When R = 0.5, the voltage dependence is also small as to be insignificant. But when R = 0.4 or less, the resistance value Rs rises as the voltage VH increases. It is believed that this is because the depletion layer has been expanded. On the other hand, when R = 0.8, the resistance value Rs goes down as the voltage VH increases. It is believed that this is because an accumulation of carriers has taken place.

[0031]

[Effect of the Invention]

As explained above, since the semiconductor device of this invention is equipped with the insulating film as well as the resistance bias electrode on the resistance layer, the expansion of the depletion layer between the semiconductor substrate and the resistance layer is suppressed. Thus, the voltage dependence of the resistance of the resistance layer can be reduced.

[0032]

The invention also has the advantage that an additional power source is not required, since the voltage applied to the resistance bias electrode layer is provided from the middle of the resistance layer in longitudinal direction.

[0033]

Furthermore, the manufacturing method of this invention allows for the reduction of manufacturing process steps, because the first silicon layer remains intact when the field oxide film is formed and then is used as a part (lower part) of the resistance bias electrode layer.

[0034]

Also, the resistance layer of the second conductivity type is formed by the ion

implantation of the impurity of the second conductivity type penetrating through the first silicon layer and the insulating film. Then, the second silicon layer is deposited on the first silicon layer. Thus, the first silicon layer functions as the buffer film against the ion implantation and the acceleration energy of the ion implantation can be reduced compared to the case in which the single silicon layer is used as the resistance bias electrode layer. [Brief Description of Drawings]

[Fig. 1] Fig. 1 is a cross-sectional view for explaining the manufacturing method of a semiconductor device according to the embodiment of this invention.

[Fig. 2] Fig. 2 is a cross-sectional view for explaining the manufacturing method of the semiconductor device according to the embodiment of this invention.

[Fig. 3] Fig. 3 is a cross-sectional view for explaining the manufacturing method of the semiconductor device according to the embodiment of this invention.

[Fig. 4] Fig. 4 is a cross-sectional view for explaining the manufacturing method of the semiconductor device according to the embodiment of this invention.

[Fig. 5] Fig. 5 is a cross-sectional view for explaining the manufacturing method of the semiconductor device according to the embodiment of this invention.

[Fig. 6] Fig. 6 is a cross-sectional view for explaining the semiconductor device and its manufacturing method according to the embodiment of this invention.

[Fig. 7] Fig. 7 is a plan view of the diffusion resistance shown in Fig. 6.

[Fig. 8] Fig. 8 is another plan view of the diffusion resistance shown in Fig. 6.

[Fig. 9] Fig. 9 (A) - 9 (C) are graphs showing the current-voltage characteristics and the resistance characteristics of the diffusion resistance (the difference in the voltages between the both sides of the diffusion resistance being shown on the X-axis, and the electric current I and the resistance Rs being shown on the Y-axis).

[Fig. 10] Fig. 10 (D) - 10 (F) are graphs showing the current-voltage characteristics and the resistance characteristics of the diffusion resistance (the difference in the voltages between the both sides of the diffusion resistance being shown on the X-axis, and the electric current I and the resistance Rs being shown on the Y-axis).

[Fig. 11] Fig. 11 is a cross-sectional view of a semiconductor device of the prior art.

[Fig. 12] Fig. 12 is a cross-sectional view showing the semiconductor device of the prior art in use.

[Document Name] Abstract

[Abstract]

[Subject] This invention is directed to the reduction of voltage dependence of a resistance layer and thus allows easy design of integrated semiconductor circuits.

[Solving Means] The device is equipped with a P^--type resistance layer 8, in which a first voltage VL is applied to one end and a second voltage VH is applied to the other end and which is formed on the surface of an N-well region 2 on the semiconductor substrate, a thin oxide film 3 on the resistance layer 8, and a resistance bias electrode layer 10 which includes the silicon layer formed on the thin oxide film 3. By adjusting the voltage applied to the resistance bias electrode layer 10, the voltage dependence of the resistance of the resistance layer 8 is reduced.

[Selected Figure] Fig. 6